Office of the Dean Research and Consultancy
Indian Institute of Engineering Science & Technology (IIEST), Shibpur Howrah-711103

Project on: "Design and Development of System on Chip based next Generation IoT System for Industry 4.0 with Functional Safety and Security Features"

[Sponsoring Authority: Chip to Startup (C2S), MeitY, Govt. of India]

School of VLSI Technology
Indian Institute of Engineering Science & Technology (IIEST), Shibpur Howrah-711103

Ref.: Advt. No. VL 1874, dated 17.09.2025

[University Project Code: DRC/MEITY-C2S(4197)/VLSI/HR/005/23-24]

Interested candidates are requested to appear for walk-in interview on **09.10.2025 at 11:00 am** for the following post in the School of VLSI Technology Department, Indian Institute of Engineering Science & Technology (IIEST), Shibpur, Howrah-711103

Name of the Post: Project Associate - I

No. of Post: - 2

Essential Qualification: M.Tech / B.Tech (having 1 years of experience in Analog and Mixed Signal Design) with 8.0 CGPA along with institute norms.

Remuneration: INR 30,000/- per month (Consolidated)

Desirable Qualification (s):
Experience with Analog and Mixed Signal Design, FPGA, Coding, chip tape-out and IC testing.

Experience / Software / Skillset:
Experience in Analog and Mixed Signal Design, Design knowledge of low power design, knowledge of RISC-V, experience in chip tape out, product design, and testing. Knowledge of VLSI EDA Tools, Verilog, RTL coding, and Functional Coding using C, Verilog-A and MATLAB.

Job Descriptions:
- ✓ Carry out research in IC design, testing, and product development for Industry 4.0.
- ✓ Coordinate with cluster institutes for project activities and attend training .
- ✓ Maintain EDA tools and laboratory workstations and support students in the related area.
- ✓ Create essential documentation for projects and manuals for EDA tools .
- ✓ Assisting PI's with various activities towards completion of the project.

Age Limit: Upper age limit for the manpower position will be 50 years. The service duration should not exceed beyond 60 years of age.

Duration: 3 years or until the completion of the project, subject to yearly evaluation of the candidate for the project execution.

Interested eligible candidates should mail soft copies of the application letter in plain paper, recent bio-data, marksheets, certificates research papers (if any), work experience certificate (if any), etc., in a single PDF file sent by email with "advertisement No."on the subject link to the below-mentioned e-mail ID. All documents should be self-attested. Physical documents will be verified at the time of joining. The selection will be cancelled if any discrepancies are found in the documents at the time of physical verification.

Venue of the interview: School of VLSI Technology Department, IIEST, Shibpur.

Note:
1. Soft copies of the application letter, bio-data, mark sheets and certificates should be sent through e-mail in advance by **08.10.2025 at 5:00 PM** to Prof. Hafizur Rahaman, Chief Investigator (E-mail id: hafizur@vlsi.iiests.ac.in).
2. All applications must mention a valid e-mail id and phone number for communicating date of interview.
3. Short listing may be done before the interview.

17/09/25

Dean (R & C)

(W. Code-DRC-006/25-26)

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